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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,023	02/03/2004	Jason P. Gill	BUR920030118US1	2022

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,023	GILL ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1,2,21,22,39 and 40* is/are rejected.

7)☒ Claim(s) *3-20 and 23-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/3/04 & 3/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 39 and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 39 contains the phrase "a source drain implanted into the gate structure" line 6 of the claim. The examiner is unable to find this limitation within the specification. Thus the examiner believes that the applicant intended to describe a structure which has a gate on a substrate and has a source and a drain at the sides of the gate electrode.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Manning et al. (USPN 5,232,865).

6. In reference to claims 1 and 21, Manning et al. (USPN 5,232,865, hereinafter referred to as the "Manning" reference) discloses a similar process and device. Figures 6 and 13 of Manning each illustrate a semiconductor device having a contact stud (20A and 20B – figure 6, 20 – figure 13) with an integral resistor (22A and 22B – figure 6, 22 – figure 13). In both figures, there is a substrate (10) having at least one contact area. An insulating layer (16) is formed over the substrate (10) and is in contact with the contact area. There is a contact hole formed in the insulating layer (16) which exposes the contact area. A contact stud (20A and 20B – figure 6, 20 – figure 13) is disposed in the contact hole. The contact stud (20A and 20B – figure 6, 20 – figure 13) has an upper surface and a lower surface. The lower surface is in circuit connection with the contact area. An integral resistive material (22A and 22B – figure 6, 22 – figure 13) is disposed within the contact hole on at least an upper surface or a lower surface of the contact stud (20A and 20B – figure 6, 20 – figure 13) so that the resistive material and the contact stud form a local resistor structure. The method of fabricating the Manning device of figures 6 and 13 inherently meets the fabrication process described in claim 1.

7. With regard to claims 2 and 22, Manning discloses the use of silicon-implanted oxide and silicon-implanted nitride (column 3, lines 29-35). The method of fabricating the Manning device of figures 6 and 13 inherently meets the fabrication process described in claim 2.

8. Claims 1 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yang et al. (USPN 6,130,462).

9. In reference to claims 1 and 21, Yang et al. (USPN 6,130,462, hereinafter referred to as the "Yang" reference) discloses a similar process and device. Figure 12A of Yang illustrates a semiconductor device having a contact stud (220) with an integral resistor (195). There is a substrate (106A) having at least one contact area. An insulating layer (145) is formed over the substrate (106A) and is in contact with the contact area. There is a contact hole formed in the insulating layer (145) which exposes the contact area. A contact stud (220) is disposed in the contact hole. The contact stud (220) has an upper surface and a lower surface. The lower surface is in circuit connection with the contact area. An integral resistive material (195) is disposed within the contact hole on at least an upper surface or a lower surface of the contact stud (220) so that the resistive material and the contact stud form a local resistor structure. The method of fabricating the Yang device of figures 6 and 13 inherently meets the fabrication process described in claim 1.

10. Claim 39 is rejected under 35 U.S.C. 102(b) as being anticipated by Klein (USPN 6,297,083 B1).

11. So far as understood in claim 39, Klein (USPN 6,297,083 B1) discloses a similar device. Figure 2g of Klein illustrates a resistor structure. Klein makes it clear (column 3, line 67 and column 4, lines 1-6) that this structure can be utilized in conjunction with the contact (30) within the SRAM structure shown in figure 1a. The figure 1a SRAM structure illustrates an interlevel dielectric substrate (34). A gate structure (21) is formed within the interlevel dielectric substrate (34). A source (23) and a drain (24) are implanted next to the gate (21). Figure 2g

shows a contact (45) which can be formed within the source (23) and the drain (24). A first thin resistor film (47) is formed on the interlevel dielectric (42) and the contact (45). A refractory metal film (48) is deposited (column 5, lines 62-65) on the thin resistor film (47). A conductive metal (49) is deposited (column 6, lines 3-7) on the refractory metal film (48).

Allowable Subject Matter

12. Claims 19 and 20 are allowed.

13. Claims 3-20 and 23-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor memory device of the static random access memory type where the resistive material is a thin film located on a recessed contact stud (and the resistive material has a width no larger than the width of its contact hole) which is located at a cross coupling between a first metal layer cross coupling node and a polysilicon gate node at either an interface between the contact and the first metal layer interface or an interface between the contact and the polysilicon gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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